## ABSTRACT

The present invention discloses a system for buffering the outputs of peripheral devices operating in UTOPIA protocol to allow devices on separate circuit boards connected through long buses, such as backplanes, to communicate with the system controller. Address detection logic stores the peripheral device address and compares it to the UTOPIA bus address signal. When the correct address is recognized in a first clock cycle, a flip flop stores the information for the next cycle. A second flip flop stores the state of the read enable signal. An AND gate detects when the correct address was found and the read enable was de-asserted during the first clock cycle and the read enable and read cell available signals are positive during the current clock cycle and provides a high signal to a third flip flop. On a third clock cycle the third flip flop enables the outputs of a data buffer which then drives the peripheral device data signals on to the read data bus. The third flip flop output and the read enable signal are provided to a second AND gate which feeds back to the third flip flop to maintain its state until the read enable signal is de-asserted. The first flip flop is also used to control a buffer for the read cell available signal from the peripheral device. The third flip flop is also used to control a buffer for the read start of cell signal from the peripheral device.